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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LP	6,459,118 B1	10/02	Kang			
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LP	K. Noda et al., "A Boosted Dual Word-line Decoding Scheme for 256Mb DRAMs" Symposium on VLSI Circuits Digest of Technical Papers; pp. 112-113; 1992.
LP	M. Nakamura et al., "A 29ns 64Mb DRAM with Hierarchical Array Architecture" IEEE International Solid-State Circuits Conference, pp. 246-247, 1995.

EXAMINER	DATE CONSIDERED 06/23/2004

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.